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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/401,765	09/23/1999	PHILIP J. CALAMATAS	WAB98553	5126

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JAMES RAY & ASSOCIATES
2640 PITCAIRN ROAD
MONROEVILLE, PA 15146

EXAMINER
GOSSAGE, GLENN A

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.

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	6

DATE MAILED:

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on 1-15-02 ☑ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ~~days~~ from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 4-9 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☑ Claims 1-3 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 4-9 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☑ The proposed drawing correction, filed 1-15-02, has been ☑ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

☆ U.S. GOVERNMENT PRINTING OFFICE: 1995-391-982

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A new title such as --Programmable System Including Self Locking Memory Circuit For a Tristate Data Bus-- is suggested.

Note that specific instructions should be provided to change the title (not merely a new title provided at the top of a substitute specification, e.g.) so that the amended title is reflected in all appropriate places, particularly in the PALM (Patent Application Location Monitoring) system.

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on January 13, 2002 have been approved by the Examiner, subject to drafting review.

The drawings remain objected to, however, because in Figure 1A (as shown in the proposed drawing corrections filed January 15, 2002), it appears the dashed "box" for reference numeral 220 should only include one set of circuit elements 10, 12 and 26 (see page 6, lines 12-13 and 17 of the substitute specification, e.g.).

In Figure 1B (as amended), the addition of the "boxes" labeled "DSP" and "CPLD" is confusing. [How is this "DSP" related to the "DSP chip" label, e.g.? Should the added "boxes" labeled DSP and CPLD be placed within their respective "boxes," adjacent to the labels "(DSP CHIP)" and "(OTHER CHIPS)," for example?]

Applicant is again REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

The drawings are also objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the complex programmable logic device of claims 6, 8 and 9, must be shown or the features canceled from the claims. No new matter should be entered.

3. It is noted here that the substitute specification filed January 15, 2002 has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 1, line 2, it appears "co-pending" should be deleted (provisional applications are not "pending" any action).

On page 1, the penultimate (next-to-last) line, it appears --between the CPU and the processing devices-- should be (re)inserted after "transfer" for clarity and consistency with the disclosure as originally filed and to avoid possible questions of NEW MATTER.

Similarly, on page 2, line 12, it appears --gates of-- should be reinserted before "of the chip" for clarity and consistency with the disclosure as originally filed.

On page 6, line 7, it appears "Motion Control" should be moved before "Digital" for clarity and consistency (with the acronym "DSP" and page 1, lines 16-17, e.g.).

On page 7, line 8, it appears --for circuit 220-- or other similar language should be inserted after "level" for clarity and consistency (note the original specification, e.g.).

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

In the claims:

In claim 4, line 9, it appears --wherein-- should be inserted before "said" and "having" changed to --has-- for clarity (note that a new element is not being set forth here). See also claims 7 and 9, line 8.

In claim 5, lines 6-7, it appears "unit; said" should be changed to --unit, said-- (i.e., a new subparagraph should not be started) for clarity since a new claim element is not being set forth. See also claim 6, lines 7-8 (it appears "Device; said" should be changed to --Device, said-- for clarity). In line 14, it appears "--said-- should be inserted before "Digital" for clarity. See also claim 6, line 17.

In claim 6, line 3, it appears "programmable" should be --Programmable-- for consistency. In line 16, it appears "said access" reads more clearly here as simply --access--. See also claim 8, line 13. In line 17, it appears "--said-- should be inserted before "Digital" for clarity analogous to claim 5, line 14.

In claim 8, line 14, it appears "--said-- should be inserted before "Complex" for clarity.

Appropriate correction is required.

4. It is again noted here that this application appears to contain claims directed to distinct inventions.

More specifically, claim 4 sets forth a "self-locking memory circuit" for a tri-state data bus, which appears to be a subcombination of the "programmable system" of claims 5 and 8, which programmable system includes "self-locking data bus circuits." [In this regard, also see MPEP 806.05(c).] However, combination claims 5 and 8 not setting forth the details of the subcombination claim appear to provide evidence that the combination as claimed does not require the particulars of the subcombination for patentability. Additionally, the subcombination appears to have separate utility such as a self-locking memory circuit for different circuits in a computer or data processing system (in this regard, also see page 2, lines 1-5 and page 6, lines 2-5 of the originally filed specification).

Again, while these inventions appear to be distinct, a restriction requirement is NOT being made at this time since it does not appear there will be a substantial burden on the Office if restriction is not required, given that there are a limited number of claims in each group and since the searches for the different groups overlap to some extent.

However, restriction may be required in the future depending on how the claims are amended. In this regard, again see MPEP 811.

5. Claims 6-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 6, the language "system further includes ..." is confusing and not entirely clear here, as it is not readily apparent how the elements of claim 6, such as the tri-state data bus, bit lines, self locking data bus circuits, etc., are connected or related, if at all, to the elements, such as the tri-state data bus, bit lines, and self locking memory circuits, of claim 5 (again note that the elements of claim 6 are set forth in addition to the elements of claim 5).

In claim 7, the proper antecedent for "said self locking memory circuit" (see lines 8, 9-10 and 10-11, e.g.) Is not entirely clear since there are plural circuits set forth in the claim (see line 2, e.g.). Should "said" in line 8 be changed to --each--, and "said in lines 9 and 10 changed to --that--? See also claim 9, lines 8, 9 and 10.

In claim 8, and therefore claim 9 dependent therefrom, lines 5-6, "said Digital Signal Processor" has no clear antecedent here.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Buch.

With respect to claim 4, Buch discloses a "self locking" memory or bus latching circuit for a tri-state data bus having multiple bit or data lines, the memory or latching circuit including a non-inverting buffer or amplifier (64, 66 together, e.g., in Figure 5, as well as column 5, lines 58-62) for connection to one of the bit or data lines, and a resistor (68 in Fig. 5, e.g.) having a predetermined electrical resistance connected across the buffer or amplifier. [Again note that while two inverters are shown in Figure 5, Buch also specifically teaches that a non-inverting amplifier may be used in place of the pair of inverters 64, 66 (see column 5, lines 60-62, e.g.)]

The memory or bus latching circuit maintains or stores the level of data on the bus until a subsequent data or voltage level is driven onto the data bus. The resistance value may be chosen

to adjust the thresholds at which the circuit will change state. In this manner, the memory or latching circuit has upper and lower "threshold" voltage thresholds that cause the buffer chip or latching circuit to change states when a level of voltage applied to the chip and the resistor "passes through" one of the thresholds. The memory or latching circuit is "self-locking" and does not change state until a voltage is again applied to the data bus which "passes through" one of the thresholds. See column 5, lines 31-35; column 5, line 56 to column 6, line 2; column 6, line 61b to column 7, line 5; and Figure 5, for example..

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buch.

Buch discloses a "programmable" computer system including a tri-state data bus electrically connected to a central processing unit (CPU), and a plurality of "self-locking" data bus latching or memory circuits connected to respective bit or data lines of the data bus. Buch teaches that the "self locking" data bus latching circuit may include a non-inverting buffer or amplifier and a resistor having a predetermined electrical resistance connected across the buffer or amplifier (see

numbered paragraph 6 above, e.g.), so that the data bus latching circuit maintains or stores the level of data on the bus until a subsequent data or voltage level is driven onto the data bus In this way, different components of the computer system operating at different rates may communicate over the data bus, while maintaining data integrity and allowing faster bus switching times.

Buch teaches that the bus may be a communication link between one or more computer components, and that the various components of the computer system may be "nodes" comprised of large scale integrated circuits or chips (see column 1, lines 14-39, e.g.), but does not specifically teach that the large scale integrated circuits or chips or components of the system are comprised of a digital signal processor (DSP) and a complex programmable logic device (PLD) having different rates at which they operate in performing their respective functions than that of the CPU.

However, Bush does teach that the components may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g.), and it would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made to utilize large scale integrated circuit components or chips such as a digital signal processor and complex programmable logic device as circuit components or chips, which are commonly used with data buses, in conjunction with the self-locking circuits of Buch, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow appropriate communication between the different chips. It would have been obvious to

use such data bus latching circuits because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a computer or communication system (note column 1, line 55 to column 2, line 64, e.g.).

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chiang et al is again noted of particular interest as disclosing a bus hold or latch circuit including a pair of inverters, which form a non-inverting buffer, and a resistor connected across the buffer, similar to the present invention, and as also specifically teaching using such a data bus hold or latch circuit with programmable logic devices (PLDs) such as complex PLDs (CPLDs) as in the present invention (see column 1, lines 13-54 and Fig. 1, e.g.).

9. Applicant's arguments filed January 15, 2002 have been considered but are not persuasive.

With respect to claim 4, the argument that the self locking memory circuit as now claimed includes a non-clocked, non-inverting amplifier (response at page 8) is not persuasive because Buch clearly teaches that the self locking memory circuit may include a non-clocked, non-inverting amplifier (see column 5, lines 58-62, e.g.).

With respect to claims 5-9, the argument that Buch does not specifically teach the interconnection of a CPU with either or both of a DSP and a CPLD through the tri-state data bus having self-locking data bus circuits (response at page 8) is not persuasive because Buch teaches that the bus may be a communication link between one or more computer components, and that the various components of the computer system may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g., as well as column 1, lines 14-39).

One of ordinary skill in the art at the time the claimed invention was made would have found it readily obvious to utilize typical components as taught by Buch, such as a digital signal processor (which is merely a processor which processes digital signals) and a "complex" programmable logic device which are large scale integrated circuit components or chips commonly used with data buses, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow appropriate communication between the different chips. It would have been obvious to use such data bus latching circuits because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a computer or communication system (note column 1, line 55 to column 2, line 64, e.g.).

A requirement that Buch specifically mention DSPs and CPLDs as the typical components to be used is tantamount to requiring a reference to anticipate the claimed invention under 35

U.S.C. 102. Here, the reduction or avoidance of delays due to transitions in a tri-state bus and accompanying improvement in data bandwidth and integrity, coupled with the teaching of using the self-locking data bus circuit in conjunction with typical computer components and large scale integrated circuits commonly used with data buses, as taught by Buch, provide ample motivation and suggestion to utilize the self-locking data bus circuits of Buch in conjunction with computer components commonly used with data buses such as DSPs and CPLDs. Thus, the proposed modification is not arrived at merely through applicant's own disclosure as contended by applicant (response at page 9) but is based on the teachings and motivation provided by the reference.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2